IN THE CLAIMS

1. (Currently amended) A data storage apparatus comprising a scrambling circuit for converting ~~an~~ a plurality of input ~~signal~~ signals respectively representing test results for a plurality of elements to a desired format, and a storage device for storing converted data;

wherein said scrambling circuit includes:

a plurality of conversion circuits for respectively ~~each~~ converting said ~~input signal~~ plurality of input signals according to different rules; and

a selector for selecting one of signals output by said plurality of conversion circuits and supplying what is selected to said storage device.

2. (Original) A data storage apparatus comprising a scrambling circuit for converting an input signal to a desired format, and a storage device for storing converted data;

wherein said scrambling circuit is constituted by a rewritable device.

3. (Original) The data storage apparatus according to claim 2, wherein said scrambling circuit includes:

a plurality of conversion circuits each converting said input signal according to different rules; and

a selector for selecting one of signals output by said plurality of conversion circuits and supplying what is selected to said storage device.

4. (Original) The data storage apparatus according to claim 1 wherein said scrambling circuit includes a digital signal processor for processing an output signal of an AD converter.

5. (Original) The data storage apparatus according to claim 2 wherein said scrambling circuit includes a digital signal processor for processing an output signal of an AD converter.

6. (Original) The data storage apparatus according to claim 3 wherein said scrambling circuit includes a digital signal processor for processing an output signal of an AD converter.

7. (Original) The data storage apparatus according to claim 1 wherein said scrambling circuit includes an automatic address generation circuit for automatically generating address signals for identifying storage locations in said storage device in response to externally supplied commands.

8. (Original) The data storage apparatus according to claim 2 wherein said scrambling circuit includes an automatic address generation circuit for automatically generating address signals for identifying storage locations in said storage device in response to externally supplied commands.

9. (Original) The data storage apparatus according to claim 3 wherein said scrambling circuit includes an automatic address generation circuit for automatically generating address signals for identifying storage locations in said storage device in response to externally supplied commands.

10. (Original) The data storage apparatus according to claim 1 wherein said scrambling circuit includes a compression circuit for compressing retrieved data from said storage device into a desired format and for outputting the compressed data.

11. (Original) The data storage apparatus according to claim 2 wherein said scrambling circuit includes a compression circuit for compressing retrieved data from said storage device into a desired format and for outputting the compressed data.

12. (Original) The data storage apparatus according to claim 3 wherein said scrambling circuit includes a compression circuit for compressing retrieved data from said storage device into a desired format and for outputting the compressed data.

13. (Original) A data measuring apparatus comprising:

a data storage apparatus according to claim 1; and

a tester for testing a semiconductor device and for supplying said scrambling circuit with results of the testing.